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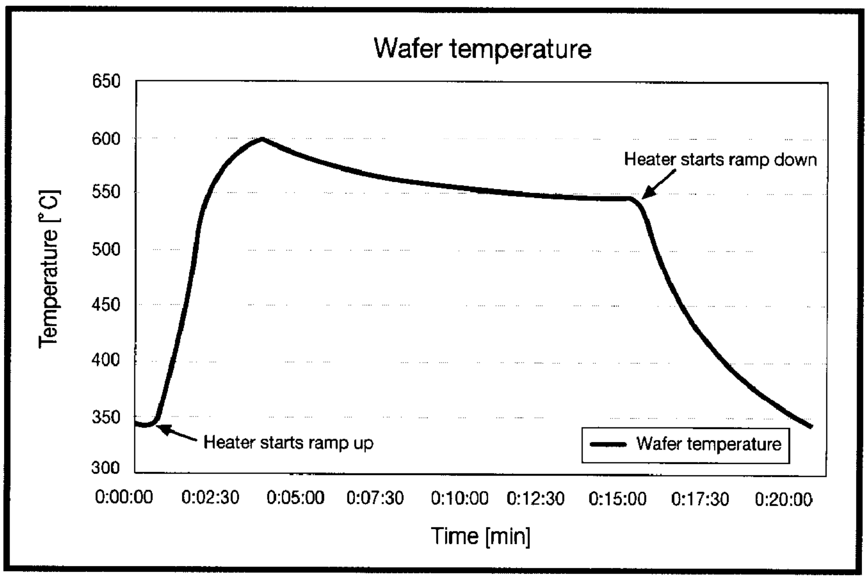
Motivated by the need to grow fast high quality virtual substrates (VS) for strained Si / SiGe channels or for Ge/GaAs applications, Unaxis Semiconductors has developed low energy plasma processes (LEPP) which are running on a new LEPP 300 cluster tool. The system combines the utilisation of plasma for pre-epi clean and for epitaxial growth in a production system. It consists of two new processes both applicable for 300 mm wafers: the LEPC (low energy plasma cleaning) process, a dry low temperature (≤150 °C) process for wafer cleaning before epitaxial growth (pre-epi clean), and the LEPECVD (low energy plasma enhanced CVD), a deposition process which allows deposition rates in the range between 0.01 nm/s and several nm /s at 550°C.

Low energy plasma processing (LEPP) for SiGe applications

Homo epitaxial growth at low temperatures on silicon substrates Low temperature epi growth is an important issue in Si and SiGe technology. Usually, there is a trade-off between substrate temperature (deposition rate) and material properties of the deposited layers (morphology, islanding, pseudomorphic or relaxed growth, Ge segregation and diffusion, dopant incorporation). The optimisation of this process depends strongly on the Ge concentrations of the layers to be produced. The utilisation of plasma enhancement allows higher deposition rates at lower temperatures.

Figure 1. The wafer reaches the required process temperature of 550°C in less than two minutes



However, for epilayers the energy of the particles in the plasma must be controlled to prevent damage to the single crystalline structure of the wafer surface. Homo epitaxial growth is very sensitive to this if it is performed at low temperatures and best demonstrates the capabilities of this process. The process approach to growing homo and hetero epitaxial layers on silicon wafers is based on a process sequence consisting of only two process steps.

The wafers are loaded from the supplier's wafer box to the cassette of the handling system. No prior wet chemical treatment of the wafers is required (such as RCA cleaning or HF dip). The wafer is then transferred from the cassette station to the LEPC module. The LEPP 300 system has a GX 8000 Brooks handling platform for wafer transport between cassette stations and the different modules. During the first process step in the LEPC module, the wafer is cleaned in an argon/hydrogen plasma at temperatures below 100°C. Typical process parameters for this step are argon and hydrogen flows of about 100 sccm, a discharge current of 50 A and low discharge voltages of about 20 V. The working pressure is in the 10- 3 mbar range.

The time to clean the wafer from the protective oxide is about 120 s. After cleaning, the wafer is

Item 300mm wafers	Initial specification
Deposition rate at 500°C substrate temperature	0.5 to 5 nm/sec
Ge relaxed thickness uniformity on 300mm at 1 sigma	10%
SiGe relaxed uniformity in thickness and deposition at1 sigma	for [Ge] <20%: 15%
Interface contamination for C and O	< 1011 / cm2
Metal contamination	< 1011 / cm2
Density of threading dislocations on Si epi at 550°C	< 10011 / cm2
B doping for >30% SiGe alloy	up to 5x1019 / cm3
As doping for >30% SiGe alloy	1018 / cm3
SiGe threading dislocation density	for [Ge] < 20%: <105 dis/cm2
Added particles > 0.3 µm per Ø 200mm wafer for a SiGe (10%)	< 100
Ge 200mm wafers	
Thickness uniformity	10%
SiGe threading dislocation density	for [Ge] 100%: <108 dis / cm2

transferred to the LEPECVD module onto the wafer heater being already at temperatures between 400°C and 500°C. The wafer is reaching the required process temperature of 550°C in less than two minutes (see Figure 1) and the plasma is initiated. Thanks to the low energy characteristics of the plasma, the wafer can be directly exposed to the plasma. This increases the hydrogen desorption and the surface mobility of the atoms during the deposition process. In addition, the high electron density in the discharge has a 50 A discharge current, which helps to dissociate the precursors efficiently.

This ensures high deposition rates and increases the utilisation of the precursors, which is of particular importance for expensive gases like germane. In a typical deposition process the working gas flow (argon) is 80 sccm and the discharge current 150 A at a discharge voltage below 20 V. The wafer is heated to a temperature of about 550°C and the reactive gas flow (only silane in this case) is 90 sccm. Homo epitaxial growth with rates of 2.5 nm/s are routinely obtained under these conditions. Figure 2 shows a SEM photograph of the cross section of an Si epilayer. The thickness of this layer is about 1.0 µm. There is, as expected, no indication of an interface in the SEM photograph and no difference in morphology between the epilayer and the wafer.

The x-ray rocking curve of the (004) reflex of this epilayer is shown in comparison to the corresponding reflex of the bare wafer in Figure 3. This intensity measurement demonstrates the good quality of the epilayer. Although

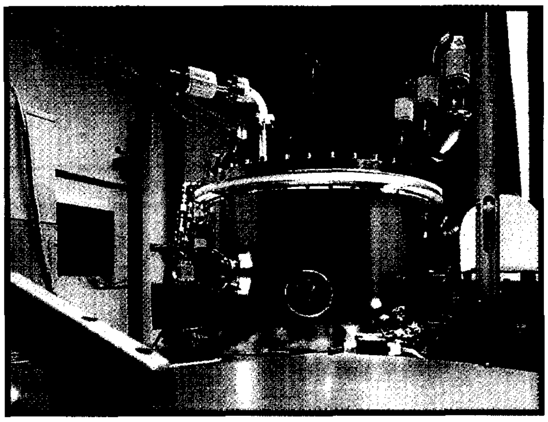


Figure 2. SEM photograph of the cross section of an Si epilayer. The thickness of this layer is about 1.0 µm.

Rutherford Backscattering Spectroscopy (RBS) channeling is not as sensitive as high resolution x-ray diffraction measurements, it gives independent information about epilayer growth. Figure 4 compares the yield of the backscattered He nuclei at 2 MeV incident energy for the random and aligned orientation of the epilayer sample. The minimum yield for the spectrum obtained for the aligned sample position is

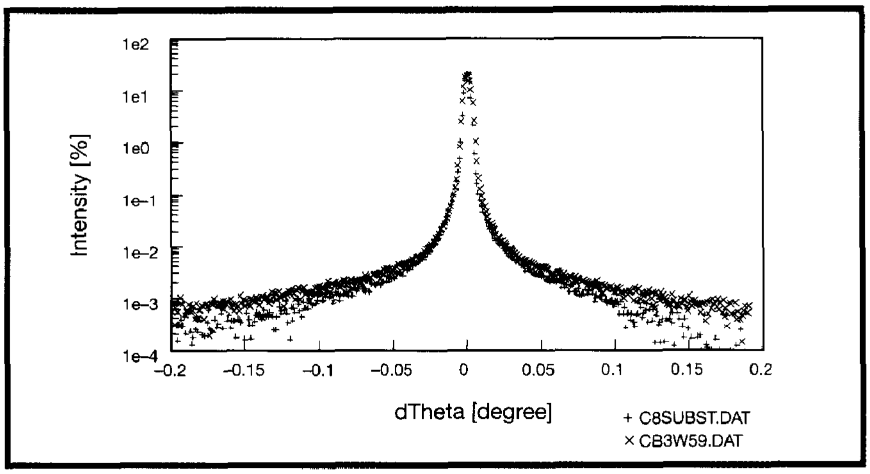


Figure 3. The x-ray rocking curve of the (004) reflex of the epilayer is shown in comparison to the corresponding reflex of the bare wafer.

about 4%, which confirms good epilayer growth. We believe this is the first time a two step dry process sequence for wafer temperatures below 600°C homo epitaxial layer growth has been realized in a production tool.

Comparison of LEPECVD growth rates with state-of-the-art LPCVD and UHVCVD processes

In SiGe technology, low temperatures during epitaxial growth are mandatory. Although the addition of germane increases the deposition rates for SiGe layer growth at lower temperatures, existing technologies such as LPCVD and UHVCVD cannot fulfill the requirements for the economical production of thick graded buffers with high germanium concentrations. The comparison of the deposition rates for homo epitaxial growth utilising silane as the precursor is especially impressive. The deposition rate for the batch-type UHVCVD process at 550°C with a silane flow of 50 sccm is 0.5 nm/min. In LPCVD, a single wafer process, homo epitaxial growth rates at 650°C are 0.3 nm/min (typical deposition at 100 Torr, 0.05 slm SiH_4, 35 slm H_2). With the 2.5 nm/s deposition rates already realized, the single wafer LEPP has 250 to 400 times higher deposition rates than conventional technology for this application.

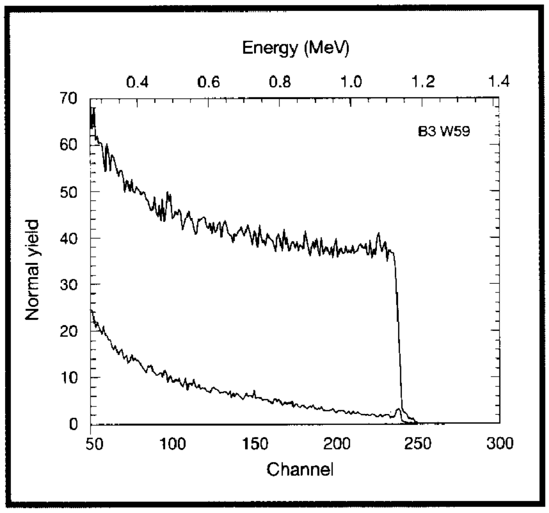


Figure 4. Comparison of the yield of the backscattered He nuclei at 2 MeV incident energy for the random and aligned orientation of the epilayer sample.

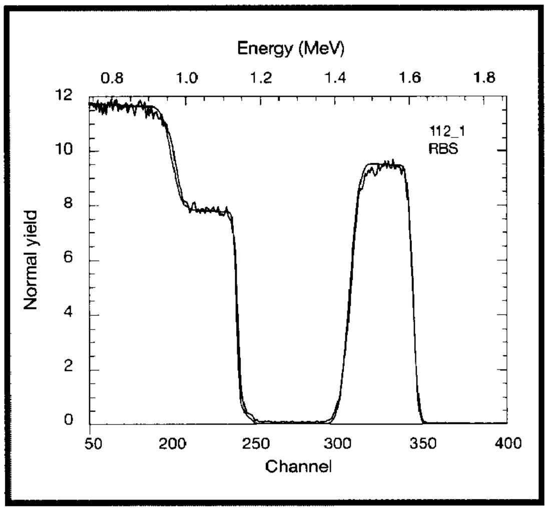


Figure 5. RBS spectrum of a SiGe layer deposited on a silicon wafer.

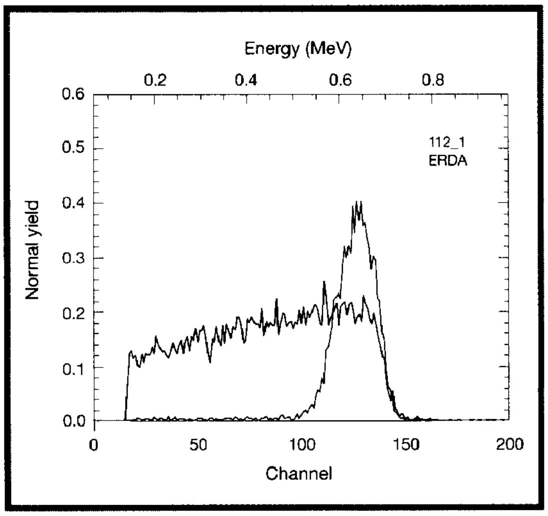


Figure 6. ERD spectrum for the same sample.

Deposition of amorphous SiGe (a-SiGe:H) layers at very low temperatures

Although the objective of the LEPP process development is low temperature epi growth of Si and SiGe, amorphous layers of SiGe may have a great potential in future CMOS technology and for MEMS applications. Therefore, we performed a short process development, for a-SiGe:H layers during the startup of the LEPP 300 system. The intention was to calibrate gas flows for the Ge incorporation in the SiGe layers at very low wafer temperatures. We used pure SiH_4 and 5% GeH_4 diluted in He as precursors for the deposition. For a constant flow of SiH_4, the flow of the diluted GeH_4 was varied between 10 sccm and 100 sccm.

Layers of about 100 nm thickness were deposited on silicon wafers which were cleaned by LEPC. The stoichiometry of the as-deposited layers was measured by RBS. In Figure 5, an RBS spectrum of a SiGe layer deposited on a silicon wafer is shown. This layer was deposited at a wafer temperature of about 80°C utilising a SiH_4 flow of 50 sccm and an effective GeH_4 flow of 5 sccm. The discharge current was set to 60 A. Under these conditions, a 20% concentration of germanium was obtained in the layer. Based on the flow ratio and our experience for epitaxial growth, only 9% Ge concentration would have been expected.

To explain the reason for this deviation, an Elastic Recoil Detection (ERD) analysis was performed for the amorphous SiGe films to determine the hydrogen concentrations in the layers. In Figure 6, an ERD spectrum is shown for the same sample. The comparison between the hydrogen depth profile and the mica standard allows an estimation of 21% hydrogen atoms in the layer. This gives some explanation for the deviation of the Ge concentration from the "theoretical" value. The calibration of the Ge incorporation in the a-SiGe:H layers as a function of the GeH4 flow is shown in Figure 7. There are two possibilities for reducing the hydrogen concentration in the a-SiGe:H films. The conventional method is an increase in wafer temperature. The other possibility, which is unique to our process, is the increase in the discharge current, i.e., the enhancement of the dissociation of the precursors and hydrogen desorption during deposition.

Future objectives for the process development of LEPP 300 VS with different Ge concentrations of up to 100% are the main objectives for the process development on the LEPP 300 tool. At Unaxis Semiconductors, this will be accompanied by an assessment on a beta-site system at a customer starting the second half of this year.

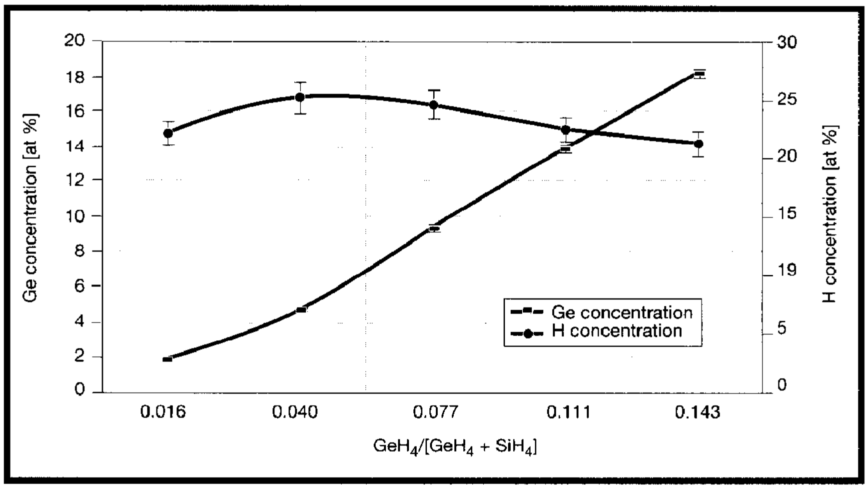


Figure 7. Calibration of the Ge incorporation in the a-SiGe:H layers as a function of the GeH4 flow

There are different levels of specifications which need to be met in the coming months. The initial specifications for the first level are listed in Table 1. The wafer sizes for the process development are 300mm for VS to support device development in the HeteroCMOS market. 200 mm wafer sizes will be used for pure Ge layers and as substrates for hetero epitaxial growth of GaAs on Ge.